# 2024 Advanced PCB Re-Make
# For the Atari 800XL
# Board Revision 1.2
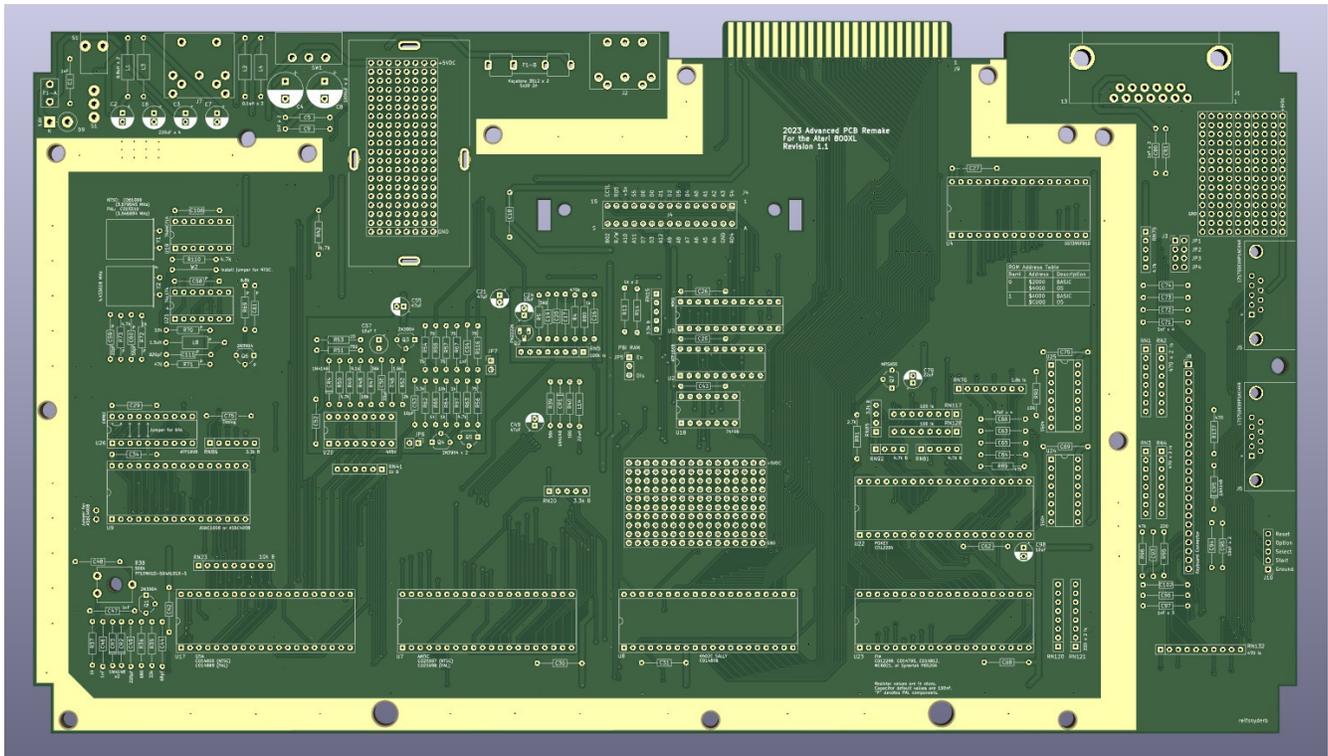


Note: The BOM has been updated from the 2023 version. However, the schematics need updated due to the addition of the MapRAM option.

Manual
Version 0.99b

By Brian E. Reifsnyder

**Contents:**

**Non-standard liability notice to satisfy lawyers:**

I, Brian E. Reifsnyder guarantee that I, personally, have assembled a board similar and/or identical to the board described within this manual and it is now a functional Atari 800XL computer. However, I do not guarantee that the board described within this manual will be useful as a computer component, paper weight, lawn ornament, or even a wall hanger. As I have no knowledge of your skills and expertise, I will not guarantee that this board will be functional once you assemble it. By doing anything with this board, you agree that I am not responsible for any bodily and/or property damage due to the assembly, non-assembly, use of, or non-use of this board. If, for example, you assemble this board incorrectly, and it turns into an indoor barbecue grill, I am not responsible for the 4 alarm fire that follows. By even casually glancing at any circuit board that is similar to the board described within this manual, you agree that you assume any and all risk associated with anything that happens or does not happen involving this board and that Brian E. Reifsnyder, his family, pets, friends, neighbors, and even his second cousin's friend's college roommate is not responsible.

**Introduction:**

Like many projects, this board has considerably evolved.  The original intent was to take the Atari 800XL system board (C061851 Revision D) and add some upgrades.  The original upgrades were as follows:

1. Chroma video output on monitor port pin 5.
2. +5VDC on PBI pins 47 and 48.
3. /HALT on PBI pin 33.
4. The optional blur capacitor (C56, 180pF) was re-added.  (Note:  This blur capacitor was later reduced to 33pF as per the video circuitry used in the Atari 800.)
5. An enhanced MMU with the following changes:
    a. Open collector PBI Refresh to prevent ANTIC's Refresh signal from being shorted out due to the actions of some PBI upgrades.
    b. PBI RAM at $D600-$D7FF.  (Inspired by Atari's original XL Sweet 16 design document.)
    c. ROM access on read only.
6. Improved DB-9 joystick ports.
7. Full copper ground planes on both sides.
8. Isolated audio and isolated video ground planes.

After some discussion, on the Atari Age forums, many additional changes were made.  These include:

1. Reduced the component count by making the following changes:
    a. Replaced all DRAM circuits with SRAM circuits.
    b. Replaced the OS and BASIC ROMs with a single chip.
    c. Combine the functions of the 74LS138 and memory control into a single PLC.
    d. Eliminate the ferrite beads and unnecessary 1nF capacitors.
    e. Simplify the power circuitry.
    f. Replace many resistors with resistor arrays and networks.
    g. Replace the audio circuit with the audio circuit designed by mytek on the AtariAge forums.
    h. Remove the RF video in favor of composite and S-Video.
    i. Use the simplified clock circuit used by mytek on the AtariAge forums.
2. Multiple memory options that include 64k only, 128k XE, and 320k RAMBO.
3. Addition of the jumpers as per Atari's original XL Sweet 16 design document.  (These are optional.)
4. Addition of three breadboard regions for user customization.
5. Channel select switch has been re-purposed as a ROM bank select switch to permit two possible OS/BASIC configurations.
6. Addition of separate pads for console keys.
7. Most components have values and/or part numbers on the board to aid in assembly and troubleshooting.
8. Addition of two locations for a fuse and a zener diode to protect against power supplies going over-voltage.  (This is experimental.)

This revision, Revision 1.2, includes the following changes:

1. The re-settable fuse was removed because there isn't a reasonable fuse rating available for this purpose.

2. A small connection breadboard was added to the left of the SIO connector to facilitate custom SIO upgrades, such as S-Drive Simple.
3. Minor video trace improvements were made to improve the layout of the video components.
4. Composite video components are now designated with a "C" on the system board.
5. +5v and GND power supply pads are now indicated on the system board.
6. The 100nF capacitor, for the cartridge, will now only provide service to the cartridge.
7. Footprints have been added for the ~20pF capacitors required for use with a non-OEM oscillator crystal.
8. A minor fix was added for on-board shielding of the clock signal near the PBI.
9. MapRAM support was added so as to gain access to the full 2k of memory located at $D000-$D7FF.

**Silkscreen Errors:**

No known errors at this time.

**Options:**

Jumper Block J3:

This jumper block has jumpers labeled JP1 through JP4 and is completely optional. All four jumpers can be permanently solder jumpered and RN75 omitted.

Note: On board Revision 1.1, RN75 doesn't specify which type of resistor network is to be installed. RN75 is a bussed resistor network.

These jumpers were added as Atari's document titled "Sweet16 Operating System External Reference Specification", page 14, describes four option jumpers as follows:

Option jumpers – There are four option jumpers provided in the hardware. The operating system shall read the states of these jumpers during power-on and store the states in data base variable JMPERS in location 030E. The bit assignments are shown below:

| Bit | Function | Hardware name |
|-----|----------|---------------|
| 0 | 0 = power-on self-test enable | J1 (pot 4). |
| 1 | unassigned | J2 (pot 5). |
| 2 | unassigned | J3 (pot 6). |
| 3 | unassigned | J4 (pot 7). |
| 4-7 | unused | N/A. |

In the two versions of the 1200XL operating system, Atari had support for J1. The 600XL and 800XL still have the jumper for J1 but support has been removed from the OS. Even so, in most XL OS revisions, Atari retained the JMPERS variable at location $030E.

This board supports these four jumpers both because these jumpers were specified within the Sweet16 specification and in the event an operating system is modified to support these jumpers.

OS's 6.4 and beyond now support J2. Removing J2 disables the Attract Mode.

MapRAM:

On all Atari 8 bit computers, the 2k memory region from $D000-$D7FF is unavailable. MapRAM was an upgrade created to permit access to this region by setting PORTB ($D301) to 0?11???0. This feature can be enabled or disabled by setting jumper JP5-"MapRAM". If you are installing either a U1MB or VBXE, this feature should be disabled. An EMMU, at U26, is required for this feature.

Oscillator:

A non Atari OEM crystal can be used for Y1 by installing two capacitors in C10 and C11. Capacitors ranging from 18pF to 22pF have been successfully used. The Y1 footprint also includes a location for the Atari OEM crystal and is designated as "OEM". Do not install C10 and C11 if using an Atari OEM crystal.

Power Supply:

The power supply section of the board has been divided into three sections:
1. Protection
2. Digital power supply
3. Audio/Video power supply

The goal is to keep any fluctuations in the digital circuitry isolated from the audio/video circuitry. The audio and video circuits each have their own 47uF capacitor as well.

In an attempt to protect the computer against any power supply failures that result in an over-voltage condition, a 5.6v zener diode (D9) can be installed. A fuse should also be installed at F1. A 2 amp fuse is recommended. The theory of operation is that in an over-voltage condition, the 5.6v zener diode will start conducting to ground. This should blow the fuse and/or power supply so as to protect the computer.

PBI RAM:

The 1400XL and 1450XLD provided 512 bytes of RAM at $D600-$D7FF for dedicated PBI device use. This feature can be enabled or disabled by setting jumper JP5-"PBI RAM". If you are installing either a U1MB or VBXE, this featured should be disabled.

RAM Options:

64k Only:

U9:  Install AS6C1008.
U26:  Do not install.  Solder 4 jumpers as per arrows on board.
C75:  Not needed.
RN86:  Not required.

64k with MapRAM:

U9:  Install AS6C1008.
U26:  Program and install ATF16V8 as the EMMU.
RN86:  Install 3.3k ohm bussed resistor SIP.

128k as 130XE configuration:

U9:  Install AS6C1008.
U26:  Program and install ATF16V8 as the EMMU.
C75:  Install a 1nF timing capacitor.  (Testing has shown this is optional.)
RN86:  Install 3.3k ohm bussed resistor SIP.

Banking is accomplished as per Atari's standard PORTB ($D301) banking for the Atari 130XE.

320k as 64k base and 256k RAMBO:

U9:  Install AS6C4008.
U26:  Program and install ATF16V8 as the EMMU.
C75:  Not required.
RN86:  Install 3.3k ohm bussed resistor SIP.
Install jumper to the left of U9.

Banking is handled via PORTB ($D301) as follows:

Enable Bank:              Bit 4 = 0
Disable Bank:             Bit 4 = 1

Bank set via bits 2,3,5,6

Bits 0,1,7 function as usual.

Note that other configurations are possible by re-programming U26.

ROM:

This board is primarily designed for use with a SST39SF010 flash ROM.  It is possible to use an SST39SF020 or SST39SF040 flash ROM by setting the solder jumpers located underneath the ROM chip.  The SST39SF020 requires one solder jumper set and the SST39SF040 requires both solder jumpers to be set.  The settings are indicated on the board.

At least one OS is required on the ROM.
BASIC is normally on the ROM but it is possible to omit BASIC or even install other
firmware in the 8k BASIC region.
Two OS/BASIC banks are possible on the flash ROM.

The OS and BASIC are installed offset to the following addresses on the flash ROM:

| | | |
|---|---|---|
| Bank: 0 | BASIC | $2000 |
| | OS | $4000 |
| Bank: 1 | BASIC | $A000 |
| | OS | $C000 |

The channel select switch (SW1) has been re-purposed for use as a bank select switch.
Looking from the front of the computer, Bank 0 is selected when the switch is in the left
position and Bank 1 is selected when the switch is in the right position.

R42 is the hold-down resistor for the ROM bank selection.  In the event that switch SW1
fails, the computer will still be able to operate from ROM Bank 0.  If only one ROM
bank is desired, switch SW1 can be omitted.  If it is desired that switch SW1 is omitted,
R42 can be replaced with a jumper.

Video:  NTSC or PAL:

All PAL components have a "P" silk screened on the board.  See the schematic diagram
for the video circuitry to add for PAL video.  For PAL video, do not install jumper W2.

## Schematic Diagrams:

Main:
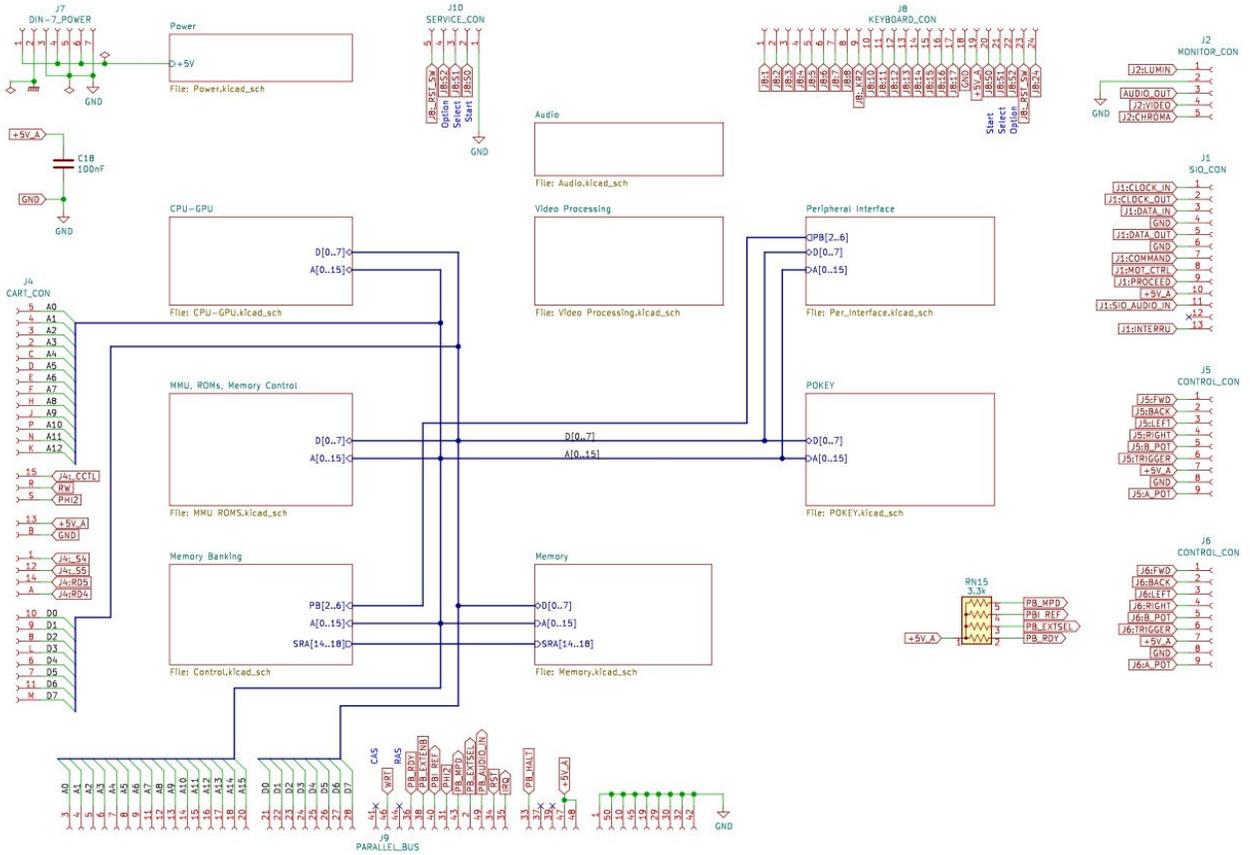
Power Supply:
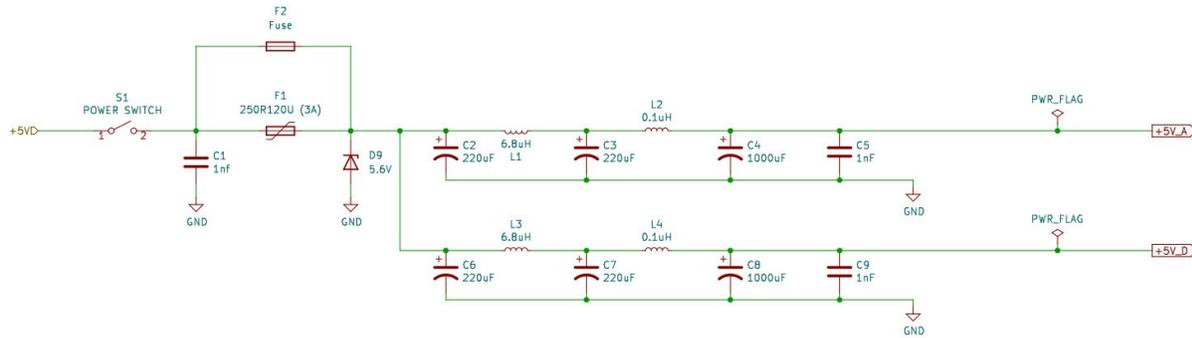


Notes:  Only one fuse is to be installed.
        F1 is for a poly fuse.
        F2 is for a 20mm x 5mm 2 AMP glass cartridge fuse.

CPU, ANTIC, GTIA:
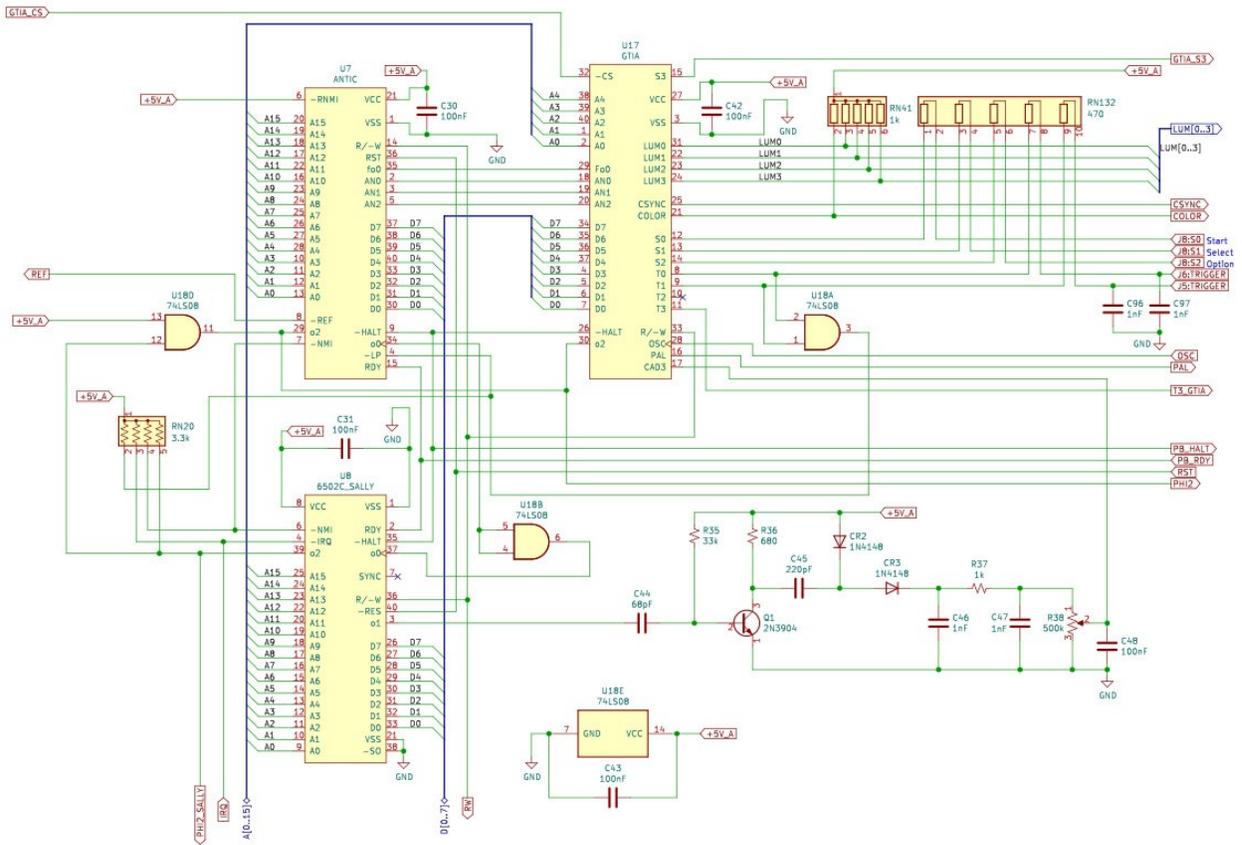


Note:  For U18, a 74F08 is recommended.

Memory Control, I/O Control, and ROM:
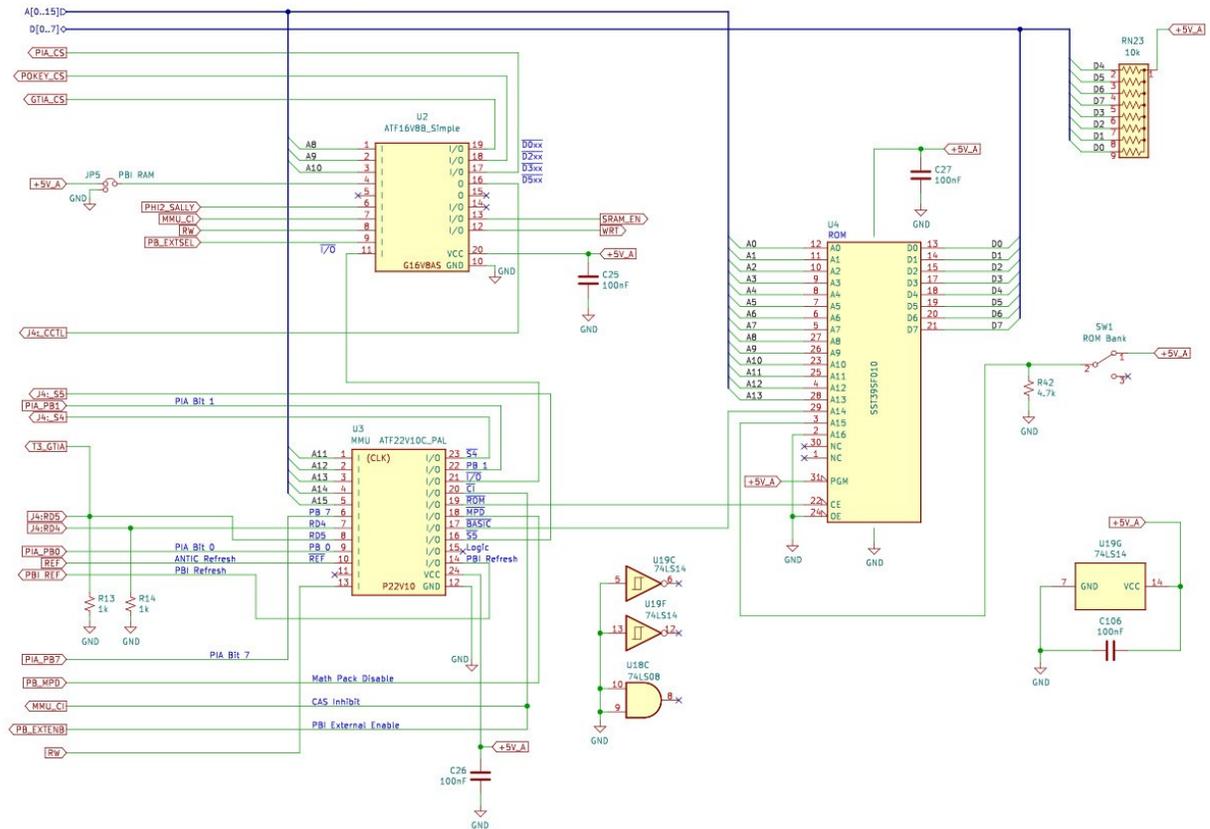


Notes: U19A must be a 74AHCT14.

EMMU:
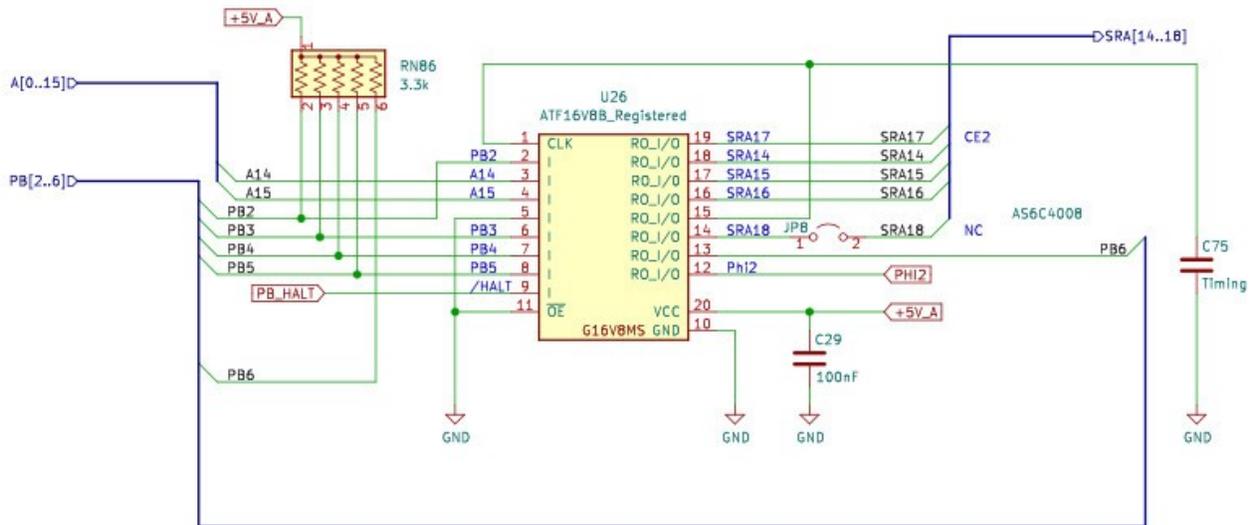


Note:  Schematic is shown for a AS6C4008 (512k) SRAM chip.  The labels of "CE2" and "NC" are for the AS6C1008 (128k) chip.  JP8, on SRA18, is only to be connected if an AS6C4008 is installed.

Memory:
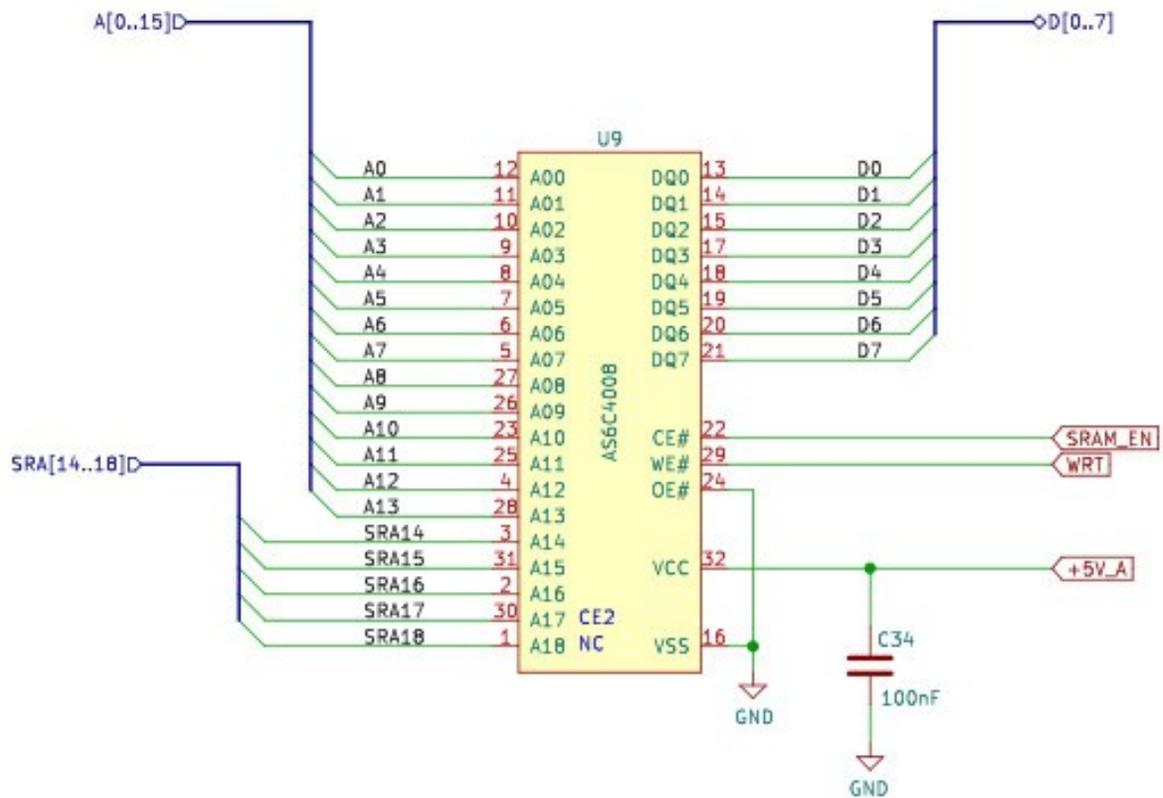


Note: If an AS6C1008 (128k) chip is used, the following pins are different:
Pin 1 – NC
Pin 30 – CE2

PIA and Reset:
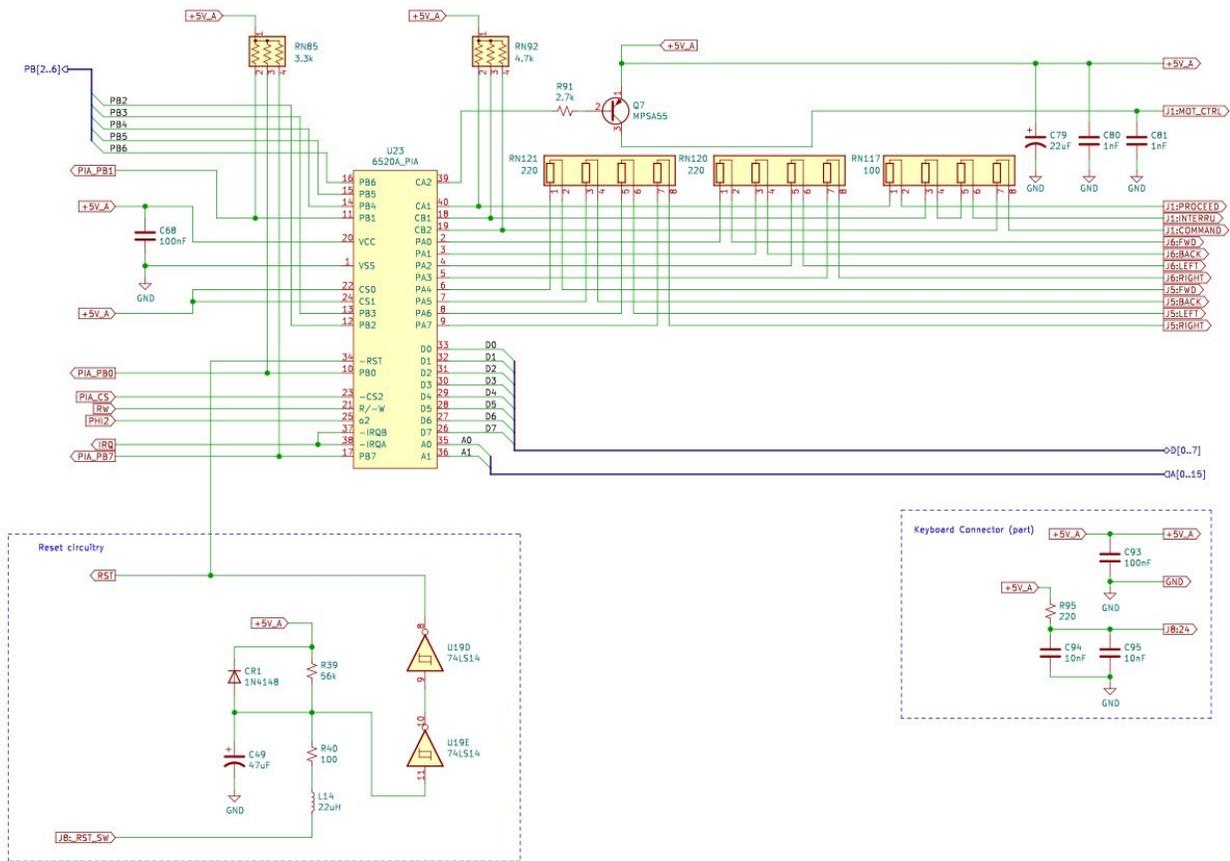


Note:   U19A must be a 74AHCT14.

POKEY and Keyboard Scan:
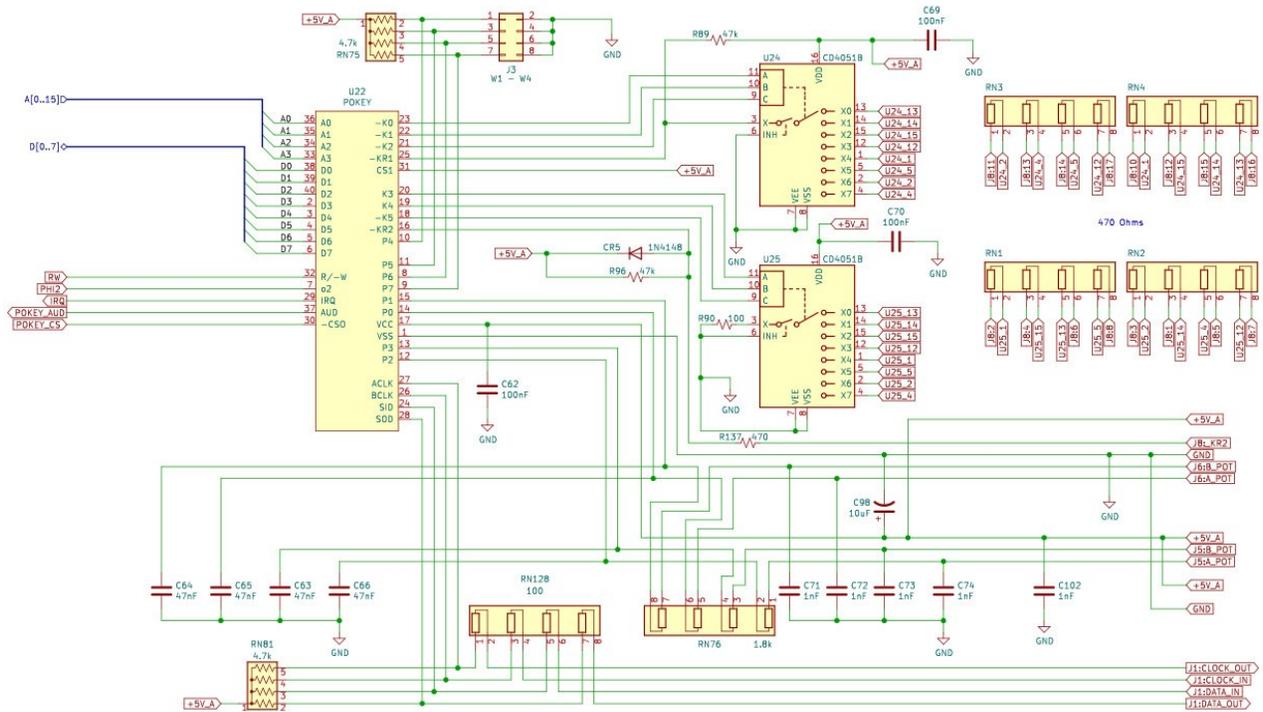


Note:  Jumper block J3 is optional.  If jumpers aren't going to be used, RN75 can be omitted and all 4 jumpers, on jumper block J3, can have permanent jumper wires soldered in.

Audio:
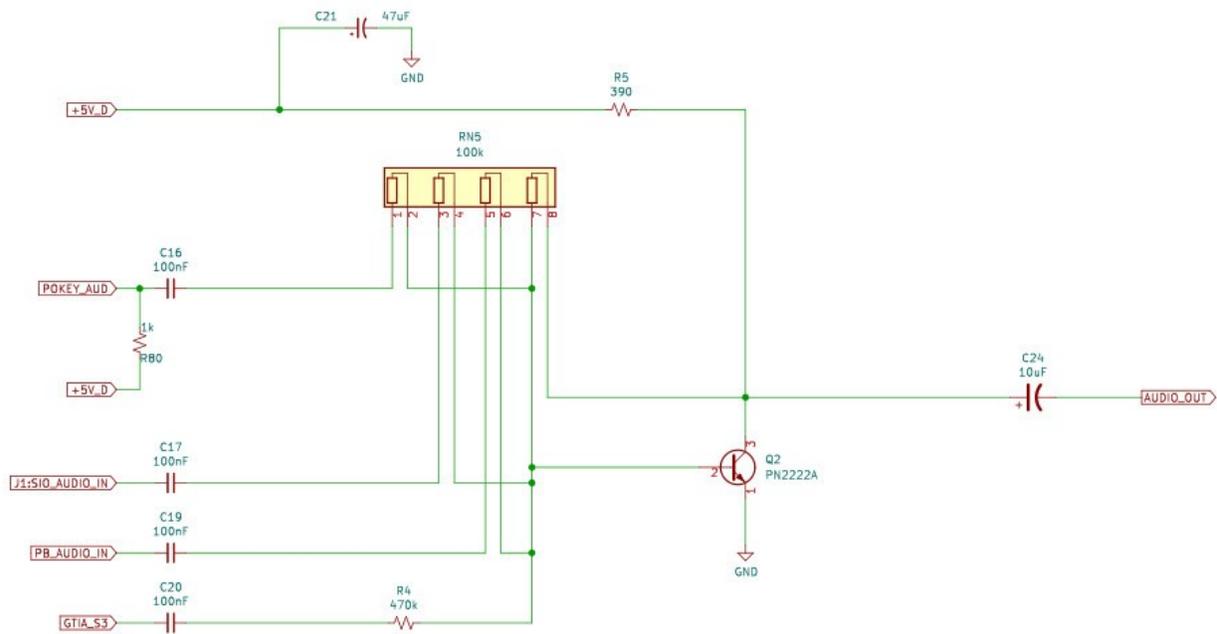


Thank you to MyTek, on the Atari Age Forums, for developing the audio circuit.

Video and Clock:
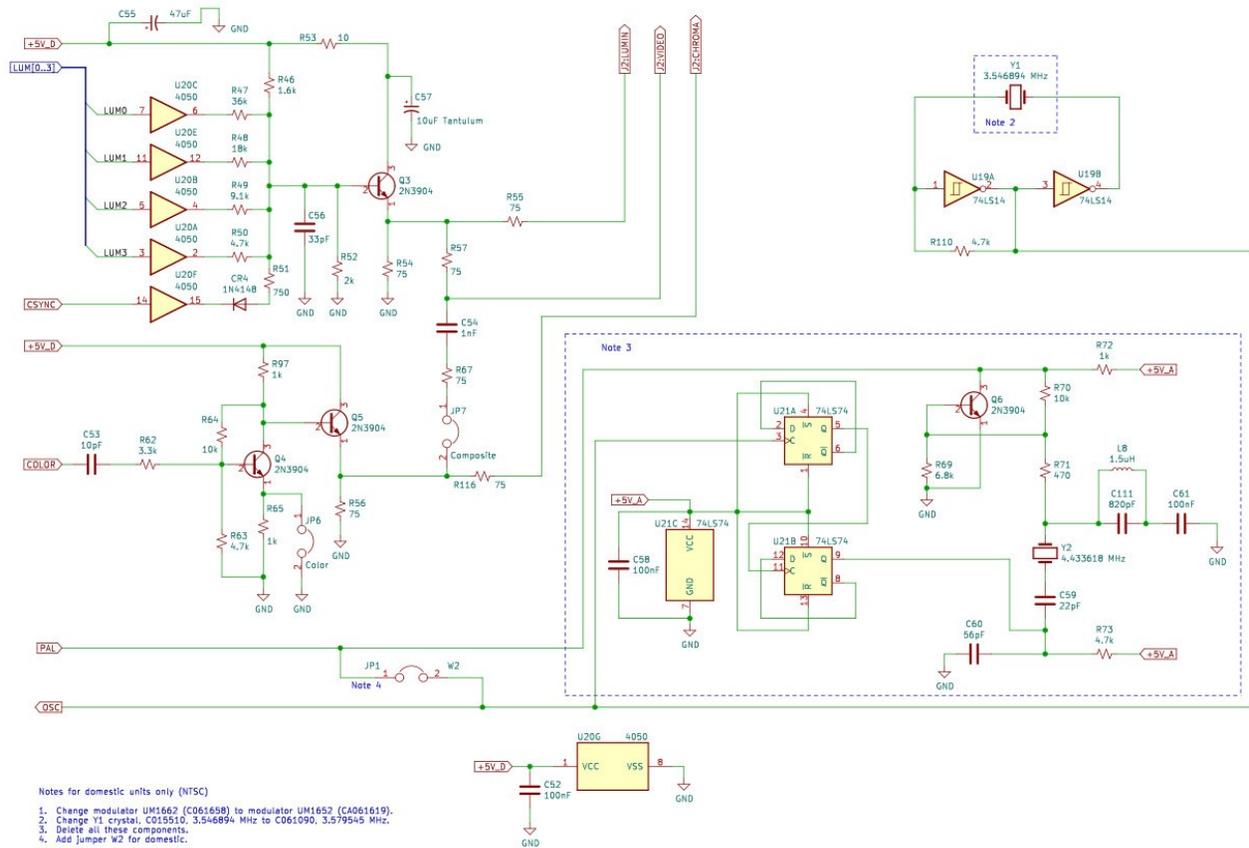


Main clock circuit developed by MyTek, from the Atari Age forums.

Notes:  U19A must be a 74AHCT14.
For composite video, install JP6 and JP7.
If composite video is never going to be used, C54, R57, and R67 can be omitted.
C56 is an optional blur capacitor.

Bill of Materials:


General Parts:


| C1, C71, C72, C73, C74, C102, C81, C46, C47, C80, C54, C97, C96, C9, C5 | | Capacitor | 1nF | |
|---|---|---|---|---|
| C10, C11 | | Capacitor | 18pF - 22pF | |
| C45 | | Capacitor | 220pF | |
| C44 | | Capacitor | 68pF | |
| C53 | | Capacitor | 10pF | |
| C56 | | Capacitor | 33pF | OB |
| C62, C69, C70, C68, C93, C48, C25, C26, C30, C31, C42, C43, C18, C52, C17, C20, C16, C19, C106, C34, C27 | | Capacitor | 100nF | |
| C63, C64, C65, C66 | | Capacitor | 47nF | |
| C75 | | Capacitor | 1nF | Mem |
| C94, C95 | | Capacitor | 10nF | |
| | | | | |
| C4, C8 | | Capacitor-D10xP5 | 1000uF | |
| C6, C2, C3, C7 | | Capacitor-D6.3x2.5 | 220uF | |
| C24 | | Capacitor-D5xP2 | 10uF | |
| C49, C55, C21 | | Capacitor-D5xP2 | 47uF | |
| C79 | | Capacitor-D5.0xP2 | 22uF | |
| C98 | | Capacitor-D5xP2.5 | 10uF | |
| | | | | |
| C57 | | Capacitor-D5xP2.5 | 10uF Tantulum | |
| | | | | |
| CR1, CR2, CR3, CR4, CR5 | | Diode | 1N4148 | |
| | | | | |
| J1 | SIO | Atari SIO Connector | | |
| J2 | MONITOR_CON | Monitor Jack | | |
| J4 | CART_CON | 30 Pin Card Edge Conn. | | |
| J5,J6 | CONTROL_CON | Joystick_Port | L717SDE09P1ACH4R | |
| J7 | DIN-7_POWER | Power_Jack | | |
| J8 | KEYBOARD | Atari Keyboard Connector | | |
| | | | | |
| JP5 | Pin Header 1x03 P2.54mm Vertical | | | |
| JP6, JP7 | Pin Header 1x02 P2.54mm Vertical | | | |
| JP5 | Pin Header 2x03 P2.54mm Vertical | | | |
| JP8 | Pin Header 1x02 P2.54 Vertical | | | |
| | | | | |
| L1, L3 | | Inductor | 6.8uH | |
| L2, L4 | | Inductor | 0.1uH | |
| L14 | | Inductor | 22uH | |

| | | | |
|---|---|---|---|
| Q1, Q3, Q4, Q5 | Transistor | TO-92 | 2N3904 |
| Q2 | Transistor | TO-92 | PN2222A |
| Q7 | Transistor | TO-92 | MPSA55 |
| | | | |
| R4 | Resistor | | 470k Ω |
| R5 | Resistor | | 390 Ω |
| R35 | Resistor | | 33k Ω |
| R36 | Resistor | | 680 Ω |
| R39 | Resistor | | 56k Ω |
| R40,R90 | Resistor | | 100 Ω |
| R46 | Resistor | | 1.6k Ω |
| R47 | Resistor | | 36k Ω |
| R48 | Resistor | | 18k Ω |
| R49 | Resistor | | 9.1k Ω |
| R50, R63, R110 | Resistor | | 4.7k Ω |
| R51 | Resistor | | 750 Ω |
| R53 | Resistor | | 10 Ω |
| R52 | Resistor | | 2k Ω |
| R54, R55, R56, R67, R116, R57 | Resistor | | 75 Ω |
| R62 | Resistor | | 3.3k Ω |
| R64 | Resistor | | 10k Ω |
| R137 | Resistor | | 470 Ω |
| R13, R14, R37, R97, R65, R80 | Resistor | | 1k Ω |
| R89, R96 | Resistor | | 47k Ω |
| R91 | Resistor | | 2.7k Ω |
| R95 | Resistor | | 220 Ω |
| | | | |
| R38 | Potentiometer 5x10 | PT10MV10-504A1010-S | 500k Ω |
| | | | |
| RN1,RN2,RN3,RN4 | SIP8 | Resistor Array, Isolated | 470 Ω |
| RN5 | SIP8 | Resistor Array, Isolated | 100k Ω |
| RN20, RN15 | SIP5 | Resistor Array, Bussed | 3.3k Ω |
| RN23 | SIP9 | Resistor Array, Bussed | 10k Ω |
| RN41 | SIP6 | Resistor Array, Bussed | 1k Ω |
| RN81 | SIP5 | Resistor Array, Bussed | 4.7k Ω |
| RN76 | SIP8 | Resistor Array, Isolated | 1.8k Ω |
| RN85 | SIP4 | Resistor Array, Bussed | 3.3k Ω |
| RN92 | SIP4 | Resistor Array, Bussed | 4.7k Ω |
| RN120, RN121 | SIP8 | Resistor Array, Isolated | 220 Ω |
| RN128, RN117 | SIP8 | Resistor Array, Isolated | 100 Ω |
| RN132 | SIP10 | Resistor Array, Isolated | 470 Ω |
| | | | |
| S1 | POWER SWITCH | E101J1AV2BE2 | |
| | | | |
| U2 Socket | DIP-20 | W7.62mm Socket | |
| U3 Socket | DIP-24 | W7.62mm_Socket | |
| U4 Socket | DIP-32 | W15.24mm Socket | |

| | | | | |
|---|---|---|---|---|
| U7 Socket | DIP-40 | W15.24mm Socket | | |
| U8 Socket | DIP-40 | W15.24mm Socket | | |
| U9 Socket | DIP-32 | W15.24mm Socket | | |
| U17 Socket | DIP-40 | W15.24mm Socket | | |
| U18 Socket | DIP-14 | W7.62mm Socket | | |
| U19 Socket | DIP-14 | W7.62mm Socket | | |
| U20 Socket | DIP-16 | W7.62mm Socket | | |
| U21 Socket | DIP-14 | W7.62mm Socket | | |
| U22 Socket | DIP-40 | W15.24mm Socket | | |
| U23 Socket | DIP-40 | W15.24mm Socket | | |
| U24 Socket | DIP-16 | W7.62mm Socket | | |
| U25 Socket | DIP-16 | W7.62mm Socket | | |
| | | | | |
| U2 | DIP-20 | GLU | ATF16V8 | |
| U3 | DIP-24 | MMU | ATF22V10 | |
| U4 | DIP-32 | ROM | SST39SF010 | |
| U7 | ANTIC | Atari LSI Chip | CO21697 (NTSC) or CO21698 (PAL) | |
| U8 | 6502C | Atari 6502C SALLY | C014806 | |
| U9 | Memory | 128k | AS6C1008 | Mem |
| U9 | Memory | 320k | AS6C4008 | Mem |
| U17 | GTIA | Atari LSI Chip | CO14805 (NTSC) or CO14889 (PAL) | |
| U18 | 74F08 | 74F08 | | |
| U19 | 74AHCT14 | 74AHCT14 | | |
| U20 | 4050 | CD4050 | | |
| U22 | POKEY | Atari LSI Chip | C012294 | |
| U23 | PIA | 6520A or equivalent | | |
| U24 | CD4051B | CD4051B | | |
| U25 | CD4051B | CD4051B | | |
| | | | | |
| Y1 | Crystal | HC49-U_Horizontal | 3.579545 MHz | NTSC |

EMMU Option (for memory other than 64k):

| | | | |
|---|---|---|---|
| C75 | Capacitor | Timing Capacitor | 1nF |
| C29 | Capacitor | | 100nF |
| RN86 | SIP6 | Resistor Array, Bussed | 3.3k |
| U26 Socket | DIP-20 | W7.62mm Socket | |
| U26 | EMMU | ATF16V8 | |

J1-J4 Jumper Option:

| | | | |
|---|---|---|---|
| J3 | Pin Header | 2x04, P2.54mm, Vertical | |
| RN75 | SIP5 | Resistor Array, Bussed | 4.7k |

PAL Video:

| | | | | |
|---|---|---|---|---|
| C58, C61 | | Capacitor | | 100nF |
| C60 | | Capacitor | | 56pF |
| C59 | | Capacitor | | 22pF |
| C111 | | Capacitor | | 820pF |
| L8 | | Inductor | | 1.5uH |
| Q6 | | Transistor | TO-92 | 2N3904 |
| R69 | | Resistor | | 6.8k Ω |
| R70 | | Resistor | | 10k Ω |
| R71 | | Resistor | | 470 Ω |
| R72 | | Resistor | | 1k Ω |
| R73 | | Resistor | | 4.7k Ω |
| U21 | 74LS74 | 74LS74 | | |
| Y1 | Crystal | HC49-U | | 3.546894 MHz |
| Y2 | Crystal | HC49-U | | 4.433618 MHz |

Power Supply:

| | | | |
|---|---|---|---|
| D9 | Zener Diode | | 5.6V |
| F2,F2 | Fuseholder Clip | 5x20mm Keystone 3512 | |
| F2 Fuse | 5x20mm | | 2A |

ROM Banking:

| | | | |
|---|---|---|---|
| SW1 | ROM Bank (was RF Switch) | | |
| R42 | | Resistor | 4.7k |

Jumpers:

Jumpers for pin headers.

## WinCupl Code for Programmable Logic Chips:

U3/MMU

```
Name      800XL 2024 Advanced PCB Remake;
Partno    NA;
Date      10/14/2024;
Revision  00;
Designer  Brian Reifsnyder;
Company   N/A;
Assembly  2024 Advanced PCB Remake - For the Atari 800XL;
Location  U3;
Device    p22v10;

/*****************************************************************/
/*   800XL 2024 Advanced PCB Remake                             */
/*   Memory Management Unit (MMU)                               */
/*   Modified from MMU code by Bob Woolley                      */
/*****************************************************************/
/*  Allowable Target Device Types: ATF22V10          */
/*****************************************************************/


/** Inputs **/

Pin 01    = A11              ; /* address bit 11                */
Pin 02    = A12              ; /* address bit 12                */
Pin 03    = A13              ; /* address bit 13                */
Pin 04    = A14              ; /* address bit 14                */
Pin 05    = A15              ; /* address bit 15                */
Pin 06    = BE               ; /* !Basic Enable                 */
Pin 07    = RD4              ; /* right cart. @ $8000-$9FFF      */
Pin 08    = RD5              ; /* left cart. @ $A000-$BFFF       */
Pin 09    = REF_ANTIC        ; /* ANTIC Refresh                 */
Pin 10    = MAP              ; /* !PB7 diagnostic bit           */
Pin 11    = REN              ; /* PB0 OS ram enable             */
Pin 13    = RW               ; /* Read/Write                    */
Pin 18    = MPD              ; /* !Math Pack Disable            */


/** Outputs **/

Pin 16    = !S5              ; /* left cart. select             */
Pin 17    = !BASIC           ; /* BASIC when low, OS w/hi       */
Pin 19    = !ROM             ; /* ROM CE                        */
Pin 20    = !CI              ; /* DRAM CAS inhibit              */
Pin 21    = !IO              ; /* I/O select @ $D000-$D7FF       */
Pin 22    = MapRAM           ; /* High when MapRAM set.         */
Pin 23    = !S4              ; /* right cart. select            */

/** Input/Output **/
Pin 14    = REF              ; /* PBI Refresh              */

/** Logic **/
Pin 15    = !OS              ; /* Macrocell for OS Logic    */
```

```
/** Logic Equations **/
/** # is or **/
/** ! is not **/

S4    = !A13 & !A14 & A15 & RD4 & REF;                          /* RD4 and addresses $8000-$9FFF */
S5    = A13 & !A14 & A15 & RD5 & REF;                           /* RD5 and addresses $A000-$BFFF */

IO    = A12 & !A11 & !A13 & A14 & A15 & REF;                    /* addresses $D000-$D7FF*/

CI    = !A13 & !A14 & A15 & RD4 & REF                           /* right cart. */
      # A13 & !A14 & A15 & RD5 & REF                            /* left cart. */
      # A13 & !BE & !A14 & A15 & !RD5 & REF                     /* BE and $A000-$BFFF */
      # OS                                                      /* OS addresses */
      # A12 & !A11 & !A13 & A14 & A15 & REF                     /* I/O addresses */
      # !REF;                                                   /* memory refresh */

MapRAM      = A12 & !A11 & !A13 & A14 & !A15                    /* MapRAM addresses $5000-$57FF */
       & !REN & !MAP & REF;

OS    = A13 & A14 & A15 & REN & REF                             /* addresses $E000-$FFFF */
      # A13 & A14 & A15 & !REN & !MAP & REF
      # !A12 & !A13 & A14 & A15 & REN & REF                     /* addresses $C000-$CFFF */
      # !A12 & !A13 & A14 & A15 & !REN & !MAP & REF
      # A12 & A11 & !A13 & A14 & A15 & MPD & REN & REF          /* addresses $D800-$DFFF */
      # A12 & A11 & !A13 & A14 & A15 & MPD & !REN & !MAP & REF
      # A12 & !A11 & !A13 & A14 & !A15 & !MAP & REN & REF;      /* addresses $5000-$5800 - mapped */

ROM   = OS & RW                                                 /* ROM CE on Read Only */
        # BASIC & RW;

BASIC = A13 & !BE & !A14 & A15 & !RD5 & REF;                    /* BE and $A000-$BFFF */

REF   = REF_ANTIC;                                              /* Simulated open collector PBI Refresh */
REF.oe = !REF_ANTIC;
```

U2

```
Name    800XL 2023 Advanced PCB Remake;
Partno   NA;
Date     11/22/2023;
Revision  00;
Designer  Brian Reifsnyder;
Company   N/A;
Assembly  2023/2024 Advanced PCB Remake - For the Atari 800XL;
Location  U2;
Device   g16v8as;

/***********************************************************/
/*   800XL 2023 & 2024 Advanced PCB Remake                 */
/*   I/O and SRAM control                                  */
/*                                                         */
```

```
/**********************************************************/
/*  Allowable Target Device Types: ATF16V8                */
/**********************************************************/


/** Inputs  **/
Pin  01  = A8            ;  /* A8                        */
Pin  02  = A9            ;  /* A9                        */
Pin  03  = A10           ;  /* A10                       */
Pin  04  = PBI_RAM       ;  /* Enable PBI RAM    (D6xx-D7FF)   */
Pin  06  = Phi2S         ;  /* Phi2 Sally                */
Pin  07  = MMU_CI        ;  /* !MMU CAS Inhibit          */
Pin  08  = RW            ;  /* RW From Sally             */
Pin  09  = PB_EXTSEL     ;  /* !EXTSEL                   */
Pin  11  = IO            ;  /* !IO                       */


/** Outputs  **/
Pin  12  = WRT           ;  /* !Write                    */
Pin  13  = SRAM_CE       ;  /* !SRAM CE                  */
Pin  16  = D5xx          ;  /* !Cartridge Control        */
Pin  17  = D3xx          ;  /* !PIA CE                   */
Pin  18  = D2xx          ;  /* !POKEY CE                 */
Pin  19  = D0xx          ;  /* !GTIA CE                  */


/** Logic Equations  **/
/** # is or **/
/** ! is not **/

!WRT          =     !RW;                                           /* RW          */

!SRAM_CE      =     MMU_CI &  PB_EXTSEL & Phi2S #                  /* RAM         */
                    !IO & A10 & A9 & PB_EXTSEL & Phi2S & PBI_RAM;  /* PBI RAM     */

!D5xx         =     !IO & A10 & !A9 & A8;                          /* CCTL        */

!D3xx         =     !IO & !A10 & A9 & A8;                          /* PIA         */

!D2xx         =     !IO & !A10 & A9 & !A8;                         /* POKEY       */

!D0xx         =     !IO  & !A10 & !A9 & !A8;                       /* GTIA        */
```

 U26/EMMU


16k Configuration:

```
Name 800XL 2024 Advanced PCB Remake;
Partno NA;
Date 10/14/2024;
Revision 00;
Designer Brian Reifsnyder;
Company N/A;
Assembly 2024 Advanced PCB Remake - For the Atari 800XL;
Location U26;
```

Device g16v8ms;

```
/*******************************************************************/
/* 800XL 2024 Advanced PCB Remake                                 */
/* EMMU - 16k Configuration                              */
/*                                                        */
/*******************************************************************/
/* Allowable Target Device Types: ATF16V8               */
/*******************************************************************/


/** Inputs **/
Pin 02 = PB2;            /* PORTB-2 */
Pin 03 = A14;            /* A14 */
Pin 04 = A15;            /* A15 */
Pin 05 = PB3;            /* PORTB-3 */
Pin 06 = PB4;            /* PORTB-4 */
Pin 07 = PB5;            /* PORTB-5 */
Pin 08 = MapRAM;         /* MapRAM */
Pin 09 = HALT;           /* !HALT */
Pin 12 = Phi2;           /* Phi2 */
Pin 13 = PB6;            /* PORTB-6 */


/** Outputs **/
Pin 15 = Pulse;          /* Clock pulse for /HALT latch. */
Pin 16 = SRA16;          /* SRAM A16 */
Pin 17 = SRA15;          /* SRAM A15 */
Pin 18 = SRA14;          /* SRAM A14 */
Pin 19 = CE2;            /* SRAM CE2 */


/** Latch **/
Pin 14 = HALTL;          /* !HALT Latch */



/** Logic Equations **/

/** # is or **/
/** ! is not **/

CE2 = !A14 & !A15;       /* Set CE2 high only when !A14 and !A15. */

SRA14 = A14;

SRA15 = A15;

SRA16 = GND;
```


64k configuration:

```
Name 800XL 2024 Advanced PCB Remake;
Partno NA;
Date 10/14/2024;
Revision 00;
Designer Brian Reifsnyder;
Company N/A;
```

```
Assembly 2024 Advanced PCB Remake - For the Atari 800XL;
Location U26;
Device g16v8ms;

/*******************************************************************/
/* 800XL 2024 Advanced PCB Remake                                  */
/* EMMU - 64k Configuration                                        */
/*                                                                 */
/*******************************************************************/
/* Allowable Target Device Types: ATF16V8                          */
/*******************************************************************/

/** Inputs **/
Pin 02 = PB2;              /* PORTB-2 */
Pin 03 = A14;              /* A14 */
Pin 04 = A15;              /* A15 */
Pin 05 = PB3;              /* PORTB-3 */
Pin 06 = PB4;              /* PORTB-4 */
Pin 07 = PB5;              /* PORTB-5 */
Pin 08 = MapRAM;           /* MapRAM */
Pin 09 = HALT;             /* !HALT */
Pin 12 = Phi2;             /* Phi2 */
Pin 13 = PB6;              /* PORTB-6 */

/** Outputs **/
Pin 15 = Pulse;            /* Clock pulse for /HALT latch. */
Pin 16 = SRA16;            /* SRAM A16 */
Pin 17 = SRA15;            /* SRAM A15 */
Pin 18 = SRA14;            /* SRAM A14 */
Pin 19 = CE2;              /* SRAM CE2 */

/** Latch **/
Pin 14 = HALTL;            /* !HALT Latch */


/** Logic Equations **/

/** # is or **/
/** ! is not **/

CE2 = A14 # !A14;                      /* Set CE2 high. */

SRA14 = A14;

SRA15 = A15 #
        A14 & !A15 & MapRAM;           /* = A15 high in 5000-57FF for MapRAM */

SRA16 = GND;

Pulse = GND;
```

128k Configuration:

```
Name 800XL 2023 Advanced PCB Remake;
Partno NA;
Date 10/14/2024;
Revision 00;
Designer Brian Reifsnyder;
Company N/A;
Assembly 2024 Advanced PCB Remake - For the Atari 800XL;
Location U26;
Device g16v8ms;


/********************************************************************/
/* 800XL 2024 Advanced PCB Remake                                   */
/* EMMU - 128k Configuration                                        */
/*                                                                  */
/********************************************************************/
/* Allowable Target Device Types: ATF16V8                           */
/********************************************************************/


/** Inputs **/
Pin 02 = PB2;              /* PORTB-2 */
Pin 03 = A14;              /* A14 */
Pin 04 = A15;              /* A15 */
Pin 05 = PB3;              /* PORTB-3 */
Pin 06 = PB4;              /* PORTB-4 */
Pin 07 = PB5;              /* PORTB-5 */
Pin 08 = MapRAM;           /* MapRAM */
Pin 09 = HALT;             /* !HALT */
Pin 12 = Phi2;             /* Phi2 */
Pin 13 = PB6;              /* PORTB-6 */


/** Outputs **/
Pin 15 = Pulse;            /* Clock pulse for /HALT latch. */
Pin 16 = SRA16;            /* SRAM A16 */
Pin 17 = SRA15;            /* SRAM A15 */
Pin 18 = SRA14;            /* SRAM A14 */
Pin 19 = CE2;              /* SRAM CE2 */

/** Latch **/
Pin 14 = HALTL;            /* !HALT Latch */


/** Logic Equations **/

/** # is or **/
/** ! is not **/

CE2 = A14 # !A14;                               /* Set CE2 high. */

SRA14 = A14 & A15 #                             /* = A14 in C000-FFFF */
        A14 & !A15 & PB4 & PB5 #                /* = A14 in 4000-7FFF when banking is off */
        A14 & !A15 & !PB4 & PB2;                /* = PB2 in 4000-7FFF when CPU banking */

SRA15 = A14 & A15 #                             /* = A15 in C000-FFFF */
        !A14 & A15 #                            /* = A15 in 8000-BFFF */
        A14 & !A15 & !SRA16 & MapRAM #          /* = A15 high in 5000-57FF for MapRAM */
        A14 & !A15 & !PB4 & PB3;                /* = PB3 in 4000-7FFF when CPU banking */
```

28

SRA16 = A14 & !A15 & !PB4;          /* Use banked RAM when 4000-7FFF and CPU banking */


## 128k as with ANTIC banking (130XE) configuration:


```
Name 800XL 2024 Advanced PCB Remake;
Partno NA;
Date 10/14/2024;
Revision 00;
Designer Brian Reifsnyder;
Company N/A;
Assembly 2024 Advanced PCB Remake - For the Atari 800XL;
Location U26;
Device g16v8ms;

/****************************************************************/
/* 800XL 2024 Advanced PCB Remake                               */
/* EMMU - 130XE Configuration                                   */
/* w/MapRAM                                                     */
/****************************************************************/
/* Allowable Target Device Types: ATF16V8                       */
/****************************************************************/

/** Inputs **/
Pin 02 = PB2;            /* PORTB-2 */
Pin 03 = A14;            /* A14 */
Pin 04 = A15;            /* A15 */
Pin 05 = PB3;            /* PORTB-3 */
Pin 06 = PB4;            /* PORTB-4 */
Pin 07 = PB5;            /* PORTB-5 */
Pin 08 = MapRAM;         /* MapRAM */
Pin 09 = HALT;           /* !HALT */
Pin 12 = Phi2;           /* Phi2 */
Pin 13 = PB6;            /* PORTB-6 */

/** Outputs **/
Pin 15 = Pulse;          /* Clock pulse for /HALT latch. */
Pin 16 = SRA16;          /* SRAM A16 */
Pin 17 = SRA15;          /* SRAM A15 */
Pin 18 = SRA14;          /* SRAM A14 */
Pin 19 = CE2;            /* SRAM CE2 */

/** Latch **/
Pin 14 = HALTL;          /* !HALT Latch */


/** Logic Equations **/

/** # is or **/
/** ! is not **/

CE2 = A14 # !A14;                    /* Set CE2 high. */
```

```
SRA14 = A14 & A15 #                        /* = A14 in C000-FFFF */
        A14 & !A15 & !SRA16 #              /* = A14 in 4000-7FFF when banking is off */
        A14 & !A15 & SRA16 & PB2;          /* = PB2 in 4000-7FFF when banking */

SRA15 = A14 & A15 #                        /* = A15 in C000-FFFF */
        !A14 & A15 #                       /* = A15 in 8000-BFFF */
        A14 & !A15 & !SRA16 & MapRAM #     /* = A15 high in 5000-57FF for MapRAM */
        A14 & !A15 & SRA16 & PB3;          /* = PB3 in 4000-7FFF when banking */

SRA16 = A14 & !A15 & !PB4 & HALTL #        /* Use banked RAM when 4000-7FFF and CPU banking */
        A14 & !A15 & !PB5 & !HALTL;        /* Use banked RAM when 4000-7FFF and ANTIC banking */

Pulse = !Phi2;                             /* Clock pulse to set HALTL latch (will have delay with timing cap) */

HALTL.d = HALT;                            /* Use SRA18 for HALTL as pin is NC for AS6C1008 */
```

## 320k as 64k base and 256k RAMBO:

```
Name 800XL 2024 Advanced PCB Remake;
Partno NA;
Date 10/14/2024;
Revision 00;
Designer Brian Reifsnyder;
Company N/A;
Assembly 2024 Advanced PCB Remake - For the Atari 800XL;
Location U26;
Device g16v8ms;

/****************************************************************/
/* 800XL 2024 Advanced PCB Remake                              */
/* EMMU - 320k Configuration                                   */
/*                                                             */
/****************************************************************/
/* Allowable Target Device Types: ATF16V8                      */
/****************************************************************/

/** Inputs **/
Pin 02 = PB2;           /* PORTB-2 */
Pin 03 = A14;           /* A14 */
Pin 04 = A15;           /* A15 */
Pin 05 = PB3;           /* PORTB-3 */
Pin 06 = PB4;           /* PORTB-4 */
Pin 07 = PB5;           /* PORTB-5 */
Pin 08 = MapRAM;        /* MapRAM */
Pin 09 = HALT;          /* !HALT */
Pin 12 = Phi2;          /* Phi2 */
Pin 13 = PB6;           /* PORTB-6 */

/** Outputs **/
Pin 14 = SRA18;         /* SRAM A18 */
Pin 15 = Pulse;         /* Clock pulse for /HALT latch. */
Pin 16 = SRA16;         /* SRAM A16 */
Pin 17 = SRA15;         /* SRAM A15 */
Pin 18 = SRA14;         /* SRAM A14 */
```

Pin 19 = SRA17;          /* SRAM A17 */

/** Latch **/

/** Logic Equations **/

/** # is or **/
/** ! is not **/

SRA14 =       A14 & A15 #                    /* = A14 in C000-FFFF */
              A14 & !A15 & PB4 #             /* = A14 in 4000-7FFF when banking is off */
              A14 & !A15 & !PB4 & PB2;       /* = PB2 in 4000-7FFF when CPU banking */

SRA15 =       A14 & A15 #                    /* = A15 in C000-FFFF */
              !A14 & A15 #                   /* = A15 in 8000-BFFF */
              A14 & !A15 & MapRAM #          /* = A15 high in 5000-57FF for MapRAM */
              A14 & !A15 & !PB4 & PB3;       /* = PB3 in 4000-7FFF when CPU banking */

SRA16 =       A14 & !A15 & !PB4 & PB5;

SRA17 =       A14 & !A15 & !PB4 & PB6;

SRA18 =       A14 & !A15 & !PB4;             /* Use banked RAM when 4000-7FFF and CPU banking */